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EXAMINER	
VAUGHAN, MICHAEL R	
ART UNIT	**PAPER NUMBER**
2131	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,027	JENNINGS, WILLIAM T.	
	Examiner	Art Unit	
	Michael R Vaughan	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-27* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-27 have been examined and are pending.

Specification

Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

The specification is objected to because of the following: on page 38, line 6 and on page 42 lines 13 and 15 there is a typo where "-" should be -- = --.

Information Disclosure Statement

An initialed and dated copy of Applicant's IDS form 1449, Paper No. 2-4, is attached to the instant Office action.

Claim Rejections - 35 USC ' 101 Utility

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 13-16, 18, and 21-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 13-16, 18, and 21 are rejected under 35 U.S.C 101 because the language of the claims 13 and 18 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment, or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC 101.

It is noted that Applicant's preamble recites an "Apparatus"; however, the body of the claim fails to recite the necessary hardware or other tangible elements to form an "Apparatus" as contemplated by §101.

Claims 22-27 are rejected under 35 U.S.C. 101 because the language of the claims 22 and 25 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment, or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC 101.

To expedite a complete examination of the instant application the claims rejected under 35 USC 101 (nonstatutory above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Objections

Claims 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 20 is similar to claim 11 but is dependent from claim 18 which is rejected under 35 USC 101 and 112 second paragraph, so consequently it is rejected and not objected.

Claim Rejections - 35 USC ' 112, second paragraph

Claims 5-8, and 13-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 is rejected to because the limitation "a third storage circuit in a feedback loop coupled to the fourth full adder" creates ambiguity to the structure of the fourth full adder. The fourth full adder has two inputs. The question arrives when one considers the third storage circuit in feedback. Generally speaking a feedback loop is created by channeling an output signal from a component back into an input port of the component. One uncertainty that is created by this feedback loop is the number of input to the fourth full adder. Does this mean the fourth full adder has three inputs? Clarification and/or correction are required. The language of the disclosed feedback loop in claim 19 is clearly stated.

Claims 13-27 are rejected to because independent claims 13, 18, 22, and 25 all contain variables that are not defined in the claim. The inclusion of variables without defining their purpose creates an uncertainty and does not adequately define the scope of the invention.

Claims 13 and 22 is rejected to because it contains a typo "nout – nin" which should be --nout = nin --.

Claims 18 and 25 are rejected to because it contains a typo "Xout –" which should be -- Xout = --.

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-10, 12-16, 18, 19, 21-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Kornerup (A Systolic, Linear-Array Multiplier for a Class of Right-Shift Algorithms).

As per claim 5, Kornerup teaches a two-dimensional dependency array of selectively coupled cells, wherein each cell comprises: a first full adder receiving a first input signal, a second input signal, and a clock signal; a second full adder receiving a third input signal, a fourth input signal, and a clock signal; a third full adder receiving au1 output of the second full adder, a fifth input signal, and an output of the first full adder, and providing an output signal; a fourth full adder receiving an input from the first full adder, an input from the second full adder and providing an output to the first full adder; a first storage circuit coupled between the second full adder and the third full adder; a second storage circuit coupled between the fourth full adder and the first full

adder; and a third storage circuit in a feedback loop coupled to the fourth full adder (Figure 6 on page 895).

As per claim 13, Kornerup teaches an apparatus for multiplication of modular numbers, comprising: a plurality of locally related cells coupled in a two-dimensional dependency array (893); and an input-to-output transfer relationship for the coupled cells given by:

Xout = (Xin + xj * ni + ai * bj + tin) mod 2,

Cout = (Xin + Xj * ni + ai * bj + tin) dlv 2,

xj = Xin mod 2,

aout = ain,

bout = bin

nout = nin

Any apparatus configured with the claimed features would be functionally able to execute the claimed calculation steps.

As per claim 18, Kornerup teaches an apparatus for multiplication of modular numbers, comprising: a multiplication stage comprising a plurality of locally related cells coupled in a two-dimensional dependency array (page 893); a reduction stage comprising a plurality of locally related cells coupled in a two-dimensional dependency array (page 896), wherein the reduction stage couples to the multiplication stage; and

an input-to-output transfer relationship for the coupled cells in the multiplication stage and the reduction stage given by:

Xout = (Xin + xj * nk + cin) mod 2,

cout = (Xin + xj * nk + cin) div 2,

xj = Xin mod 2,

nout = nin.

Any apparatus configured with the claimed features would be functionally able to execute the claimed calculation steps.

As per claim 22, Kornerup teaches an method for multiplication of modular numbers, comprising: a plurality of locally related cells coupled in a two-dimensional dependency array (893); and an input-to-output transfer relationship for the coupled cells given by:

Xout = (Xin + xj * ni + ai * bj + tin) mod 2,

Cout = (Xin + Xj * ni + ai * bj + tin) dlv 2,

xj = Xin mod 2,

aout = ain,

bout = bin

nout = nin (pages 894-895).

As per claim 25, Kornerup teaches an apparatus for multiplication of modular numbers, comprising: a multiplication stage comprising a plurality of locally related cells

coupled in a two-dimensional dependency array (page 893); a reduction stage comprising a plurality of locally related cells coupled in a two-dimensional dependency array (page 896), wherein the reduction stage couples to the multiplication stage; and an input-to-output transfer relationship for the coupled cells in the multiplication stage and the reduction stage given by:

Xout = (Xin + xj * nk + cin) mod 2,

cout = (Xin + xj * nk + cin) div 2,

xj = Xin mod 2,

nout = nin (pages 894-895).

As per claim 6, Kornerup teaches a reduction circuit coupled to the two-dimensional dependency array and sequentially receiving signals therefrom (page 893).

As per claim 7, Kornerup teaches said reduction circuit comprises a row by column array of selectively coupled cells (page 893).

As per claim 8, Kornerup teaches the two-dimensional dependency array of selectively coupled cells comprises a binary multiplier, and the reduction circuit

comprises concurrent reduction sequentially receiving signals from the binary multiplier (page 896).

As per claims 9 and 19, Kornerup teaches a serial array of interconnected cells each comprising:

a first full adder receiving a, first input signal, a second input signal, and a clock signal; a first storage circuit coupled in a feedback loop between an output of the first full adder and an input thereto; a second storage circuit receiving the first input signal and providing an output signal; and a third storage circuit coupled to the first full adder and the second storage circuit and providing an output to the adjacent cell (Figure 4 on page 894).

As per claim 10, Kornerup teaches adjacent cells are interconnected in a serial adder configuration (page 894).

As per claim 12, Kornerup teaches a first serial shift register having as an output a signal coupled to the first cell in the serial configuration; a second serial shift register providing the second input to the first full adder of the first cell in the serial configuration; and a third serial shift register serially receiving an output from the third storage circuit of the last serial adder in the serial configuration and providing a parallel output signal (page 896).

As per claims 14 and 23, Kornerup teaches a signal flow graph connecting to the cells coupled in the two-dimensional dependency array (page 893).

As per claim 15, Kornerup teaches the two-dimensional dependency array comprises a row-by-column configuration of selectively coupled cells (page 893).

As per claim 16, Kornerup teaches the two-dimensional dependency array comprises groups of two-dependency graph cells coupled together to add within one pair of cells product terms of equal weight (page 893).

As per claim 21, Kornerup teaches the multiplication stage two-dimensional dependency array and the reduction stage two-dimensional dependency array each comprises a row-by-column configuration of selectively coupled cells (page 893 and 896).

As per claim 24, Kornerup teaches coupling the plurality of locally related cells comprises coupling the cells to a near neighbor cell (page 894).

As per claim 26, Kornerup teaches coupling the first plurality of locally related cells and the second plurality of locally related cells comprises coupling the cells of each plurality in a row-by-column configuration of selectively coupled cells (page 896).

As per claim 27, Kornerup teaches coupling the first plurality of locally related cells and the second plurality of locally related cells comprises coupling cells together to add within one pair of' cells product terms of equal weight (page 893).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kornerup in view of Morita (USP 5,073,870).

As per claim 1, Kornerup teaches an apparatus for multiplication of modular numbers, comprising: a two-dimensional dependency array of selectively coupled cells (page 892-893). Kornerup does not explicitly teach the exactly disclosed circuit of claim 1. Morita does disclose the circuit of claim 1 (figure 9(a)). Morita teaches a fast additive circuit of radix number 4. Kornerup teaches a circuit with radix number 2, but states that it is very straightforward to see that the same structure can be used at a higher radix (page 894). Therefore one of ordinary skill in the art would know how to implement a radix number 4 structure into the system of Kornerup if it were necessary to achieve the results of a radix number 4 multiplication system.

In view of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the teaching of Morita within the system of Kornerup because it could allow the system to be substantially upgraded in order to perform at higher frequencies of calculation. One skilled in the art would have been motivated to generate the claimed invention with a reasonable expectation of success.

As per claim 2, Kornerup teaches the two-dimensional dependency array comprises a row by column configuration of selectively coupled cells (page 892).

As per claim 3, Kornerup teaches the two-dimensional dependency array comprises groups of two-dependency graph cells coupled together to add within one pair of cells product terms of equal weight (page 893).

As per claim 4, Kornerup teaches a binary number reduction circuit sequentially coupled to the output of the two-dimensional dependency array of cells (page 896).

As per claim 17, the examiner supplies the same rationale for the motivation as recited in the rejection of claim 1 to incorporate the radix 4 circuit of Morita within the system of Kornerup.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R Vaughan whose telephone number is 703-305-0354. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MV
Michael R Vaughan

Examiner

Art Unit 2131

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